REMARKS

The indicated allowability, over the art, of claims 4-12, 17-25 and 43 is noted, with thanks. However, it is believed that all of the presently-pending claims are allowable over the art, as will be discussed below.

Considering first the rejection of claims 1-3, 13-16, 26 and 45 as obvious from Dingwall in view of Tanaka, in the rejection, the Examiner refers to col. 5, lines 25-45 of Dingwall in which Dingwall said "…, even if the charge begins to dissipate and the brightness begins to fade,…" The Examiner considers that this statement of Dingwall corresponds to the feature of "discharging charges of the gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time" recited in claim 1. However, the Examiner is not correct.

The present invention has a feature that charges of the gradation pixel data written in the holding capacitor are discharged through the drive transistor. Due to this feature, the present invention has an advantageous effect that the variation in characteristics of the drive transistor is compensated to reduce the variation in luminance.

Specifically, the feature of "discharging charges of the gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time" as specified in claim 1 corresponds to the inventive operation in the time period (i.e., set discharge time) between time t2 and time ts, which is shown in FIG. 8 of the present application. Source voltage VS changes in this time period due to the discharge operation through the drive transistor, and the change in source voltage VS causes change in voltage (VG-VS) across the capacitor. The operation between time t2 and time ts is explained in detail in pages 18 to 21

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of the specification with reference to FIGs. 8, 9, 14 and 15. The inventive operation between time t2 and time 5s compensate variations in operational characteristics of a plurality of drive transistors to reduce the variation in luminance among a plurality of pixels.

On the contrary, Dingwall does not teach the operation between time t2 and time ts o the present invention. Dingwall only teaches the feature that write operation is carried out for a holding capacitor when a selection transistor is turned on. If the gradation pixel data written in the holding capacitor is discharged in Dingwall, this discharge is caused by a leak current of the selection transistor or the like. Therefore, Dingwall cannot compensate the variations in the operation characteristics of the drive transistors.

In the rejection the Examiner refers to paragraphs 31, 40 and 41 of Tanaka (US2001/007447) and states that Tanaka disclosed the predetermined time being less than a frame time. However, Tanaka does not teach the above feature corresponding to the operation between time t2 and time ts in the present invention. The combination of Dingwall and Tanaka does not suggest the present invention even if Tanaka teaches a predetermined time for discharging which is less than a frame time.

In addition, the Examiner states "the frame time includes a writing period and a driving period. It is obvious that discharging occurs during the driving period." However, as described in paragraph 32 of Tanaka, the holding capacitor of Tanaka is a nonvolatile data holding section composed of a ferroelectric capacitor and can hold the control data of the MOS transistor in a floating state. Since the holding capacitor is made of the ferroelectric capacitor, it is doubtful that discharging occurs in the drive period in Tanaka. Thus, no combination of Dingwall and Tanaka reasonably could be said to teach or suggest independent claims 1, 14 or 45.

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As to claim 2, the hold capacitor in the present invention holds a voltage between the second gate electrode and the second source electrode. On the contrary, the capacitor of Dingwall holds a voltage between two positions corresponding to the second power line and the gate electrode. Location of the hold capacitor in the present invention is quite different from that of Dingwall.

Therefore, independent claims 1, 14 and 45, and claims 2-3, 2, 13, 15, 16 and 26, which depend thereon cannot be said to be obvious from Dingwall in view of Tanaka.

Turning to the rejection of claim 44 as obvious from Dingwall in view of Ikeda, claim 44 is similar to claim 45. The deficiencies of Dingwall vis-à-vis 45 are discussed above. Ikeda does not supply the missing teachings to Dingwall to achieve or render obvious claim 44. Ikeda teaches the constitution in which an organic EL element is connected to a drive transistor in parallel. On the contrary, the pixel display element of the present invention is serially connected to the drive transistor. Although the capacitor holds a voltage between the gate and the source in each of the present case and Ikeda, the voltage at the source of the drive transistor changes in accordance with the progress of discharging in the present invention as shown in potential VS in FIG. 8 which the voltage at the source is fixed in Ikeda. Dingwall also discusses the fixed source voltage configuration.

Since the drive transistor and the EL element are connection in parallel in Ikeda, the current from the current source 24 is divided to the EL element 20 and transistor 24. In this configuration, if the characteristics of a plurality of drive transistors vary, the currents flowing through the EL elements of the respective pixels also vary and the variation in luminance among a plurality of pixels occurs.

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The advantageous effect of the present invention is obtained in the case that the drive transistor and the EL element are connected in serial and the capacitor is connected across the gate and the source of the drive transistor.

Therefore, claim 44 is unobvious from Dingwall in view of Ikeda.

The foregoing Amendment makes no claim changes and thus should be entered as a matter of right.

Having dealt with all the objections raised by the Examiner, the application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event further fees or charges are due, the Commissioner is authorized to charge our deposit acccount (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Patent Office via the electronic filing procedure on June 7, 2010.

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